Amendments to the Specification:

Please replace paragraph [0014] with the following amended paragraph:

According to the claimed invention, a method of accessing data from an LPC memory and a firmware memory comprises~~: receive~~ receiving an input signal that comprises a memory flag[[;]] and accessing data from the LPC memory or the firmware memory according to the memory flag.

Please replace paragraph [0025] with the following amended paragraph:

As long as the kind of memory is confirmed, one memory of the same kind is selected in step 380. In a computer system, the number of firmware memories is not limited to only one, so in step 380 one memory in a plurality of LPC memories or in a plurality of firmware memories has to be designated. In step 480, an address from the input signal is received and the address for the location of accessing data from the LPC memory or the firmware memory is latched. In step 580 an address confirmation is performed. Because the input signal consists of a plurality of 1s and 0s, if this digital signal is not checked, an incorrect signal can easily lead to errors. Step 580 confirms the input signal represents the memory address. As long as the confirmation is finished, either the subsequent step 680 is performed or the process returns to step 180~~ is returned to~~.

Please replace paragraph [0027] with the following amended paragraph:

Please refer to Fig.7. Fig.7 illustrates a computer system 30 according to the present invention. The computer system 30 is used to access data of an LPC memory and a firmware memory. The computer system 30 comprises an address storage unit 32, an interface circuit 34, an LPC ~~memory38~~ memory 38, and a firmware memory 40. The interface circuit 34 further comprises a flag reading unit 36. The function of the interface circuit 34 is to connect the address storage unit 32, the LPC memory 38 and the firmware ~~memory40~~ memory 40. The interface circuit 34 also determines a next action to be

executed according to an input signal. At first, the interface circuit 34 receives a trigger signal from an input signal and resets all instructions recorded in the interface circuit 34. Then, the flag reading unit 36 in the interface circuit 34 reads a signal "memory flag " from the input signal. The signal "memory flag" designates the LPC memory 38 or the firmware memory 40 for accessing data. The interface circuit 34 contacts the LPC memory 38 or the firmware memory 40 according to the signal of "memory flag".

Please replace paragraph [0028] with the following amended paragraph:

The address storage unit 32 receives and latches an address from the input signal. The address represents the location of the accessing data in the LPC memory 38 or the firmware memory 40. The interface circuit 34 performs a confirmation procedure for the address stored in the address storage unit 32. Then, the flag reading unit 36 reads a signal "accessing flag", which determines reading or writing action for the designated memory. Finally, the interface circuit reads data or writes data in the LPC memory 38 or the firmware ~~memory40~~ memory 40 according to the address latched in the address storage unit 32 and the signal in the flag reading unit 36.